Supplemental Notice of Allowability	Application No. 09/742,723	Applicant(s) SUSKA, MARK	
	Examiner Nelson D. Hernandez	Art Unit 2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *5/26/2005*.

2. ☒ The allowed claim(s) is/are *1-14 and 16-22*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This Office Action is made to replace the statement of reasons for indication of Allowable Subject Matter in the previous Notice of Allowability.

Allowable Subject Matter

2. Claim **1** is generic and allowable. Accordingly, the restriction requirement as to the encompassed species is hereby withdrawn and claims **6-14**, directed to the species of Fig. 2 and claims **18-22**, directed to the species of Figs. 6 and 7 are no longer withdrawn from consideration since all of the claims to this species depend from or otherwise include each of the limitations of an allowed generic claim.

3. **Claims 1-14 and 16-22** are allowed.

4. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 1, the primary reason for indication of allowable subject matter is because the prior art or a combination of prior art fails to teach or reasonably suggest a memory for storing imaging array data and clocking signals at a rate determined by the clocking signals.

Lee, US Patent 6,721,008 B2 discloses an integrated semiconductor imaging circuit (Fig. 3) (Fig. 3) for use with an electronic processing system comprising: an imaging array sensor (Fig. 3: 12) having an array of sensing pixels and an array address generator (Fig. 3: 16) integrated on a die (Fig. 3: 10); a circuit for controlling the transfer of the data from the memory at a rate determined by the processor system, and an interface (Fig. 3: 89) integrated on the die for receiving data from the imaging array sensor as determined by the imaging array sensor and adapted to transfer the data to the electronic processing system (Fig. 3: 80) as determined by the electronic processing

system (Col. 4, line 66 – col. 5, line 57). The interface transferring the data to the electronic processing system in inherently taught by Lee since the processing system (Fig. 3: 80) works at a predetermined rate.

Li, US Patent 6,833,862 B1 teaches an imaging circuit (Fig. 2) comprising a sensor array (Fig. 2: 12), a bus interface (Fig. 2: 54) with a data bus (Fig. 2: 20) for transmitting data to a processing system (Fig. 2: 18) (Col. 2, lines 32-64; col. 3, lines 13-21).

However, the teaching of Lee and Li either alone or in combination fails to teach or reasonably suggest a memory for storing imaging array data and clocking signals at a rate determined by the clocking signals.

Regarding claim 16, the primary reason for indication of allowable subject matter is because the prior art or a combination of prior art fails to teach or reasonably suggest a memory for storing imaging array data and address signals at a rate determined by the imaging array sensor.

Lee, US Patent 6,721,008 B2 discloses an integrated semiconductor imaging circuit (Fig. 3) (Fig. 3) for use with an electronic processing system comprising: an imaging array sensor (Fig. 3: 12) having an array of sensing pixels and an array address generator (Fig. 3: 16) integrated on a die (Fig. 3: 10); a circuit for controlling the transfer of the data from the memory at a rate determined by the processor system, and an interface (Fig. 3: 89) integrated on the die for receiving data from the imaging array sensor as determined by the imaging array sensor and adapted to transfer the data to the electronic processing system (Fig. 3: 80) as determined by the electronic processing

system (Col. 4, line 66 – col. 5, line 57). The interface transferring the data to the electronic processing system in inherently taught by Lee since the processing system (Fig. 3: 80) works at a predetermined rate.

Li, US Patent 6,833,862 B1 teaches an imaging circuit (Fig. 2) comprising a sensor array (Fig. 2: 12), a bus interface (Fig. 2: 54) with a data bus (Fig. 2: 20) for transmitting data to a processing system (Fig. 2: 18) (Col. 2, lines 32-64; col. 3, lines 13-21).

However, the teaching of Lee and Li either alone or in combination fails to teach or reasonably suggest a memory for storing imaging array data and address signals at a rate determined by the imaging array sensor.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson D. Hernandez whose telephone number is (571) 272-7311. The examiner can normally be reached on 8:00 A.M. to 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thai Tran can be reached on (571) 272-7382. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nelson D. Hernandez
Examiner
Art Unit 2612

NDHH
September 19, 2005